Module cla\_4bit (

Input [3:0] A, B,

Input Cin,

Output [3:0] Sum,

Output Cout

);

Wire [3:0] G, P; // Generate and Propagate

Wire [4:0] C; // Carry wires

Assign G = A & B; // Generate

Assign P = A ^ B; // Propagate

Assign C[0] = Cin;

Assign C[1] = G[0] | (P[0] & C[0]);

Assign C[2] = G[1] | (P[1] & G[0]) | (P[1] & P[0] & C[0]);

Assign C[3] = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) | (P[2] & P[1] & P[0] & C[0]);

Assign C[4] = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) |

(P[3] & P[2] & P[1] & G[0]) |

(P[3] & P[2] & P[1] & P[0] & C[0]);

Assign Sum = P ^ C[3:0];

Assign Cout = C[4];

Endmodule